IN THE DRAWINGS

Replacement sheets for drawings Figure 1A, 1B, 2, 3, 4A, 4B, 4C, and 5 are included here within.

REMARKS

Claims 1-32 are pending.

Claims 1-32 are rejected.

I. REJECTION UNDER 35 U.S.C. § 102

The Examiner rejected Claims 1-16 under *35 U.S.C. § 102(b)* as being anticipated by U.S. Patent No. 5,309,344 to *David Smith* (hereafter "*Smith*").

For a reference to anticipate a claimed invention, the reference must disclose every aspect of the claimed invention. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

Claim 1 is directed to a multiphase buck converter system with peak current sharing comprising a first buck converter coupled to a first regulator input voltage and a second buck converter coupled to a second regulator input voltage. The Examiner states that *Smith* teaches Claim 1 while citing that the system of *Smith* comprises a first converter coupled to an input voltage 801 and a second converter coupled to the same input voltage 801. Clearly *Smith* does not teach the cooperative relationship between the first two elements of Claim 1 of the present invention.

In Claim 1 of the present invention, the first buck converter generates a first converter output voltage in response to a first ON-time pulse set to a first logic state with a first start signal and a second logic state with a first stop signal and the second buck converter generates a second converter output voltage in response to a second ON-time pulse set to a first logic state with a second start signal and the second logic state with a second stop signal. The Examiner states that *Smith* teaches these elements and states that the first converter generates the output voltage 802 and the second converter generates the same output voltage 802. See Figure 8 where the first converter 100 and the second

converter 100' have outputs coupled together. Clearly *Smith* does not teach the cooperative relationship between the first two elements of Claim 1 of the present invention.

The present invention while supplying energy from two converters to a common load does not recite that the output and input of the two converters are directly coupled in common. The Abstract of *Smith* states " the two active-clamp ZVS converters are coupled in parallel to one another at their respective inputs and outputs, and are operated in a manner which reduces the overall input and output ripple currents..." Nowhere does *Smith* state that each converter has a separate input and a separate outputs as recited in Claim 1.

In Claim 1, the first buck regulator generates a first converter output voltage that supplies energy to the common load when its first ON-time pulse has the first logic state. The first ON-time pulse is set to the first logic state by a first start signal. Further, the second buck regulator generates a second converter output voltage that supplies energy to the common load when its second ON-time pulse has the first logic state. The second ON-time pulse is set to the first logic state by a second start signal. The first and second converters are controlled by pulses (first and second ON-time pulses) whose pulse width (time between logic states) is controlled by two signals (first and second start signals and first and second stop signals). Claim 1 recites that the start circuitry generates the first and second start signals in response to a regulated voltage across said common load, a reference voltage, and the first and second ON-time pulses. The Examiner states that *Smith* teaches the start circuitry of Claim 1 and states that PWM means 910 in FIG. 8 of *Smith* is the start circuitry of Claim 1. PWM 910 receives regulated voltage 801. The Examiner states that the reference voltage of Claim 1 is Vcc in FIG. 8 of *Smith*. However, *Smith* column 45, lines 37-63 states that Vcc is the output of an internal power supply 915 for "providing a low level supply of approximately 12 volts for powering the various components of PWM means 910..." Vcc in FIG. 8 is not described as a reference voltage. Further, PWM 910 does not receive the first and second ON-time pulses as recited in Claim 1. The only other signals received by PWM 910 of *Smith* are signals

coupled to ports 106 and 106' which *Smith* describes as follows in column 28, lines 41-46:

"As such, the input and output power paths of converters 100 and 100' are coupled in parallel. Additionally, each of converters 100 and 100' includes a port 106 and 106', respectively, for providing to control means 820 a signal representative of the instantaneous input current drawn by the converter."

The Examiner states that the signals S1 and S2 generated by PWM means 910 are the first and second start signals, respectively, as recited in Claim 1. Therefore, as shown in FIG. 8, PWM means 910 generates S1 and S2 in response to the output voltage 802 and a signal representative of primary currents coupled to 106 and 106'. Therefore, PWM means 910 cannot represent the start circuitry recited in Claim 1 as asserted by the Examiner. The start circuit recited in Claim 1 generates the first and second start signals in response to a voltage across a common load, a reference voltage and the first and second ON-time pulses.

In Claim 1, the first buck regulator generates a first converter output voltage that supplies stored energy to the common load when its first ON-time pulse has the second logic state. The first ON-time pulse is set to the second logic state by a first stop signal. Further, the second buck regulator generates a second converter output voltage that supplies stored energy to the common load when its second ON-time pulse has the second logic state. The second ON-time pulse is set to the second logic state by a second stop signal. The first and second converters are controlled by pulses (first and second ON-time pulses) whose pulse width (time between logic states) is controlled by two signals (first and second start signals and first and second stop signals). Claim 1 recites that the first stop circuitry generates the first stop signal in response to the first regulated voltage across the common load and the reference voltage. The Examiner states that the first stop circuitry of Claim 1 is first control means 970 shown in FIG. 8 of *Smith*. First control means 970 of *Smith* generates output 805 and only has an input S1 which the Examiner states is the first start signal of Claim 1. Output 805 is described by *Smith* as a control bus. In column 28, lines 22-25, *Smith* states that "each control bus 805 and 806

includes a control signal for the primary switch means, first switch means, and second switch means of converter 100 and 100', respectively." Therefore, according to the reference cited by the Examiner, *Smith* teaches a first stop circuitry (first control means 970) that generates a control bus 805 in response to the start signal of *Smith* (S1). Clearly *Smith* does not teach the first stop circuitry recited in Claim 1 that generates the first stop signal in response to the first regulator input voltage and the reference voltage.

In Claim 1, the first buck regulator generates a first converter output voltage that supplies stored energy to the common load when its first ON-time pulse has the second logic state. The first ON-time pulse is set to the second logic state by a first stop signal. Further, the second buck regulator generates a second converter output voltage that supplies stored energy to the common load when its second ON-time pulse has the second logic state. The second ON-time pulse is set to the second logic state by a second stop signal. The first and second converters are controlled by pulses (first and second ON-time pulses) whose pulse width (time between logic states) is controlled by two signals (first and second start signals and first and second stop signals). Claim 1 recites that the second stop circuitry generates the second stop signal in response to a first output current for the first converter output voltage supplied to the common load, a second output current from the second converter output voltage supplied to the common load, and the first ON-time pulse. The Examiner states that the second stop circuitry of Claim 1 is second control means 999 shown in FIG. 8 of *Smith*. In FIG. 8 of *Smith*, element 999 is shown as "first control means 999." Second control means 999 of *Smith* generates output 806 and only has an input S2 which the Examiner states is the second start signal of Claim 1. Output 806 is described by *Smith* as a control bus. In column 28, lines 22-25, *Smith* states that "each control bus 805 and 806 includes a control signal for the primary switch means, first switch means, and second switch means of converter 100 and 100', respectively." Therefore, according to the reference cited by the Examiner, *Smith* teaches a first stop circuitry (second control means 999) that generates a control bus 806 in response to the second start signal of *Smith* (S2).

Clearly FIG. 8 of *Smith* alone does not teach the second stop circuitry recited in Claim 1 that generates the second stop signal in response to a first output current for the first converter output voltage supplied to the common load, a second output current from the second converter output voltage supplied to the common load, and the first ON-time pulse.

Relative to the second stop circuitry of Claim 1, the Examiner then states that FIG. 11A teaches the first output current from the first converter output voltage, the second output current from the second converter output voltage, and the first ON-time pulse. The Examiner states that (sic) "I sub s" is the first output current and (sic) "I sub s" is the second output current. The Examiner does not specifically state what he considers the first ON-time pulse in FIG. 11A.

The Applicants assumes "I_S" shown in elements 950 and 960 are what the Examiner terms "I sub s." The "I_S" terminals shown in elements 950 and 960 are coupled to elements 828 and 829 which *Smith* describes as "ports." *Smith*, column 34, lines 28-33, states that "control means 820 further includes an input port 828 coupled to port 106 of first converter 100 for receiving a signal representative of the primary current of first converter 100 and an input port 829 coupled to port 106' of second converter 100' for receiving a signal representative of the primary current of second converter 100'." *Smith* states the (sic) "I sub s" (element 950) is coupled to a signal representative of the primary current of the first converter and not the first output current from the first converter output voltage as recited in Claim 1. Further *Smith* states the (sic) "I sub s" (element 960) is coupled to a signal representative of the primary current of the second converter and not the second output current from the second converter output voltage as recited in Claim 1. The Applicants assert that the reference *Smith* cited by the Examiner does not teach all the elements their cooperative relationship as recited in Claim 1.

Therefore, the Applicants respectfully assert that the rejection of Claim 1 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments.

Claim 2 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 2 further describes the limitation of the first stop circuitry. Claim 2 states that the first stop circuitry comprises a capacitor charged by a current from said first regulator input voltage when said first ON-time pulse has said first logic state and discharged when said first ON-time pulse has said second logic state and a first compare circuitry for comparing the reference voltage to a capacitor voltage across the capacitor and generating the first stop signal, wherein the first stop signal has a first logic state when the capacitor voltage is greater than the reference voltage and a second logic state when the capacitor voltage is less than the reference voltage. The Applicants have shown that *Smith* does not teach the invention of Claim 1. As such, *Smith* cannot teach the invention of Claim 2 which further limits Claim 1.

The Examiner states that *Smith* disclose the first stop circuitry of Claim 2 and cites capacitor 956 of FIG. 11A as the capacitor recited in Claim 2. Capacitor 956 is charged by two voltages, I_S of element 950 and OUT, via resistors 957 and 955, respectively. The capacitor of Claim 2 is charged by a current from the regulator input voltage. Capacitor 956 of *Smith* is charged by "I_S", a signal representative of the primary current of first converter 100", and S1 which the Examiner has stated is the first start signal. See *Smith*, column 34, lines 28-33. Clearly capacitor 956 of *Smith* is not the capacitor recited in Claim 2. The Examiner further states that controller (sic) 90 is the first compare circuitry of Claim 2. The Applicants could not find controller 90 in FIG. 11A. Further the first compare circuitry of Claim 2 is compares the voltage across the capacitor of Claim 2 to the reference voltage of Claim 1. FIG. 11A of *Smith* does not show any circuitry coupled to the voltage across capacitor 956.

Therefore, the Applicants respectfully assert that the rejection of Claim 2 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 3 is dependent from Claim 2 and contains all the limitations of Claim 2. Claim 3 further describes the limitation of the second stop circuitry. Claim 3 recites 3 elements, (1) peak circuitry for generating a peak voltage proportional to a peak value of said first output current, (2) first sense circuitry for generating a first sense voltage

proportional to said second output current and (3) second compare circuitry for comparing said first sense voltage to said peak voltage and generating said second stop signal, wherein said second stop signal has a first logic state when said first sense voltage is greater than said peak voltage and a second logic state when said first sense voltage is less than said peak voltage. The Applicants have shown that *Smith* does not teach the invention of Claim 2. As such, *Smith* cannot teach the invention of Claim 3 which further limits Claim 2.

The Examiner states that *Smith* discloses the invention of Claim 3 and cites the following:

1) for the peak voltage (output of the error amplifier in *Smith* column 49, line 22) generated by the peak circuitry. The peak voltage of Claim 3 is a voltage generated by the peak circuitry and is proportional to a peak value of the first output current of Claim 1. *Smith*, column 49, line 22 states that "the output voltage of the error amplifier controls the pulse width at the OUT pin in the following manner. OUT is the output of element 950 from FIG. 11A. *Smith* describes element 950 as a "controller" and "error amplifier" and nowhere describes it as peak circuitry generating a peak voltage proportional to a peak value of the first output current as recited in Claim 1.

2 for the peak value (threshold level in *Smith* column 49, line 43) of the first output current. *Smith*, column 49, line 43 states "in operation, the output error voltage sets a threshold level which the voltage signal at the IS pin must reach...." *Smith* states that his threshold level is a level of the voltage at I_S, which is a signal representative of the primary current of first converter 100 and not a peak value of the first output current of Claim 1.

3) for first sense circuitry for generating a first sense voltage (V_{FB} in *Smith* FIG. 11A) proportional to the second output current. V_{FB} is a voltage received from port 827 of *Smith* in FIG. 11A. *Smith* states that the "signal at port 827, which is related to the output voltage of converter 800." See *Smith* column 45, lines 7-9. V_{FB} in FIG. 11A of

Smith is not the first sense voltage proportional to the second output current as recited in Claim 3.

4) for the second compare circuitry (controller 960 in *Smith* FIG. 11A) for comparing the first sense voltage to the peak voltage and generating the second stop signal. *Smith* does not disclose any circuitry for comparing voltages proportional to output currents.

The Applicants assert that *Smith* does not disclose the invention of Claim 3.

Therefore, the Applicants respectfully assert that the rejection of Claim 3 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 2.

Claim 4 is dependent from Claim 3 and contains all the limitations of Claim 3. Claim 4 further describes the limitation of the first sense circuitry. Claim 4 recites 2 elements, (1) a first sense resistor coupled from the output of the first converter to the common load and (2) a differential amplifier having a positive and negative input coupled to the first sense resistor and an output generating the first sense voltage. The Applicants have shown that *Smith* does not teach the invention of Claim 3. As such, *Smith* cannot teach the invention of Claim 4 which further limits Claim 3.

The Examiner states that *Smith* discloses the invention of Claim 4 and specifically cites resistors 941 and 942 in FIG. 11A of *Smith* as the first sense resistor and the "error amplifier" as a differential amplifier. First, resistors 941 and 942 constitute a voltage divider coupled across output 802 and not in series from the output of the first converter to the common load. Secondly, while *Smith* may disclose that his error amplifier is a differential amplifier, it is not coupled to generate proportional to the second output current as recited in Claim 4. See *Smith*, column 48; lines 22-24. The Applicants assert that *Smith* does not disclose the invention of Claim 4.

Therefore, the Applicants respectfully assert that the rejection of Claim 4 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 3.

Claim 5 is dependent from Claim 3 and contains all the limitations of Claim 3. Claim 5 further describes the limitation of the first sense circuitry. Claim 5 recites 3 elements, (1) a first sense resistor coupled from the output of the first converter to the common load and (2) a differential amplifier having a positive and negative input coupled to the first sense resistor and an output generating the second sense voltage and (3) a sampling circuit for tracking said second sense voltage when said first ON-time pulse has said first logic state and holding a value of said second sense voltage as said peak voltage when said ON-time pulse has said second logic state. The Applicants have shown that *Smith* does not teach the invention of Claim 3. As such, *Smith* cannot teach the invention of Claim 5 which further limits Claim 3.

The Examiner states that *Smith* discloses the invention of Claim 5 and specifically cites resistors 941 and 942 in FIG. 11A of *Smith* as the first sense resistor and the "error amplifier" as a differential amplifier. First, resistors 941 and 942 constitute a voltage divider coupled across output 802 and not in series from the output of the first converter to the common load. Secondly, while *Smith* may disclose that his error amplifier is a differential amplifier, it is not coupled to generate proportional to the second output current as recited in Claim 5. See *Smith*, column 48; lines 22-24. Third, the Examiner states that flip flop 930 that receives a clock signal and generates two phase of that clock shifted 180 degrees is the sampling circuit of Claim 5. No one of ordinary skill in the art would think that a flip flop is a "sampling circuit for tracking said second sense voltage when said first ON-time pulse has said first logic state and holding a value of said second sense voltage as said peak voltage when said ON-time pulse has said second logic state" as recited in Claim 5. The Applicants assert that *Smith* does not disclose the invention of Claim 5.

Therefore, the Applicants respectfully assert that the rejection of Claim 5 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 3.

Claim 6 is dependent from Claim 3 and contains all the limitations of Claim 3. Claim 6 further describes the limitation of the start circuitry. Claim 6 recites 3 elements, (1) a compare circuit for comparing said regulated voltage across said common load to said reference voltage and generating a gate signal having a first logic state when said reference voltage is greater than said regulated voltage and a second logic state when said reference voltage is less than said regulated voltage, (2) a first select circuit for generating said first start signal in response to said first ON-time pulse, said gate signal, said second start signal, and an initialization signal, and (3) a second select circuit for generating said second start signal in response to said second ON-time pulse, said gate signal, said first start signal, and said initialization signal. The Applicants have shown that *Smith* does not teach the invention of Claim 3. As such, *Smith* cannot teach the invention of Claim 6 which further limits Claim 3.

The Examiner states that *Smith* discloses the invention of Claim 6 and cites controllers 950 and 960 as the compare circuit of Claim 6. Controller 950 compares VFB (a portion of the output voltage at 802) to I_S, which is a signal representative of the primary current of first converter 100 and generates S1 which the Examiner states is the first start signal and not the gate signal of Claim 6 which is distinct from the first start signal of Claim 1. The Applicants assets that *Smith* does not disclose the compare circuit of Claim 6.

The Examiner then states the controller 950 of *Smith* is also a first select circuit for generating the first start signal in response to the first ON-time pulse, the gate signal, the second start signal, and an initialization signal. Controller 950 only receives VFB (voltage proportional to the output voltage 802), a clock signal φ_1 (at R/C) and a signal representative of the primary current of first converter 100 (Is) and generates S1 (which the Examiner states is the first start signal) but *Smith* states is "a first duty cycle signal."

The Examiner states that controller 960 in Fig. 11A of *Smith* is a second select circuit for generating the second start signal in response to the second ON-time pulse, the gate signal, the first start signal, and the initialization signal. Controller 960 only a clock signal φ_2 (at R/C) and a signal representative of the primary current of second converter 100' (Is) and generates S2 (which the Examiner states is the second start signal) but *Smith* states is "a second duty cycle signal." The Applicants assert that *Smith* does not teach the comparator and the first and second select circuits of Claim 6 and therefore does not disclose the invention of Claim 6.

Therefore, the Applicants respectfully assert that the rejection of Claim 6 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 3.

Claim 7 is dependent from Claim 5 and contains all the limitations of Claim 5. Claim 7 further describes the limitation of the sampling circuitry of Claim 5. The Applicants have shown that *Smith* does not disclose the sampling circuitry of Claim 5 and therefore cannot disclose the invention of Claim 7.

The Examiner states that *Smith* discloses the converter system wherein the sampling circuit comprises a capacitor (capacitors 979 and 989, see Fig. 11B) having a first terminal coupled to ground and a second terminal. *Smith* states that capacitor 979 and 989 are part of delay circuits that operate with a series resistor 977 and 978 to generate an RC time constant. No one of ordinary skill in the art would mistake an RC delay network coupled to logic gates 972 and 982 as part of the sampling circuitry of Claim 5. The Examiner then states that the first control means 970 in Fig. 11B is an electronic switch for coupling the second sense voltage to the first terminal of the capacitor when the first ON-time pulse has the first logic state, the capacitor holding the value of the sense voltage as the peak voltage when the first ON-time pulse has the second logic state. First, FIG. 11B shows no connection between capacitors 979 and 989 and first control means 970. Secondly, *Smith* does not state that his first control means 970 has any sampling functionality.

Therefore, the Applicants respectfully assert that the rejection of Claim 7 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 5.

Claim 8 is dependent from Claim 6 and contains all the limitations of Claim 6. Claim 8 further defines the first select circuitry of Claim 6. Claim 8 adds the limitation that the first select circuitry comprises a compare logic circuit for generating a compare logic signal in response to the regulated voltage across the common load, the reference voltage, and the initialization signal, an initialization pulse circuit for generating an initialization pulse in response to the initialization signal and the compare logic signal, a first logic circuit for generating the first start signal in response to the first ON-time pulse, the initialization pulse, and the second start signal, and a second logic circuit for generating the second start signal in response to the second ON-time pulse, the initialization pulse, and the first start signal. The Applicants have shown that *Smith* does not disclose the first select circuitry of Claim 6 and therefore cannot disclose invention of Claim 8 further detailing first select circuitry.

Therefore, the Applicants respectfully assert that the rejection of Claim 8 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 6.

Claim 9 is dependent from Claim 8 and contains all the limitations of Claim 8. Claim 9 further defines the compare logic circuit of Claim 8. The Applicants have shown that *Smith* does not disclose the compare logic of Claim 8 and therefore cannot disclose the invention of Claim 9 further detailing the compare logic circuit.

Therefore, the Applicants respectfully assert that the rejection of Claim 8 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 8.

Claim 10 is dependent from Claim 9 and contains all the limitations of Claim 9. Claim 10 further defines the initialization pulse circuit of Claim 9. The Applicants have shown that *Smith* does not disclose the initialization pulse circuit of Claim 9 and

therefore cannot disclose the invention of Claim 9 further detailing the initialization pulse circuit.

Therefore, the Applicants respectfully assert that the rejection of Claim 10 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 9.

Claim 11 is dependent from Claim 10 and contains all the limitations of Claim 10. Claim 11 further defines the first logic circuit, introduced in of Claim 8, from which Claim 10 indirectly depends. The Applicants have shown that *Smith* does not disclose the first logic circuit of Claim 8 and therefore cannot disclose the invention of Claim 11 further detailing the first logic circuit.

Therefore, the Applicants respectfully assert that the rejection of Claim 11 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claims 8 and 10.

Claim 12 is dependent from Claim 10 and contains all the limitations of Claim 10. Claim 12 further defines the second logic circuit, introduced in of Claim 8, from which Claim 10 indirectly depends. The Applicants have shown that *Smith* does not disclose the second logic circuit of Claim 8 and therefore cannot disclose the invention of Claim 12 further detailing the second logic circuit.

Therefore, the Applicants respectfully assert that the rejection of Claim 12 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claims 8 and 10.

Claim 13 is dependent from Claim 4 and contains all the limitations of Claim 4. Claim 13 further defines the differential amplifier in the first sense circuit of Claim 4. A transconductance amplifier is one that converts a voltage differential into a current source output. Nowhere does *Smith* mention "a transconductance differential amplifier." The Applicants have shown that *Smith* does not disclose the first sense circuit of Claim 4 and

therefore cannot disclose the invention of Claim 13 further detailing the differential amplifier in the first sense circuit.

Therefore, the Applicants respectfully assert that the rejection of Claim 13 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 4.

Claim 14 is dependent from Claim 5 and contains all the limitations of Claim 5. Claim 13 further defines the differential amplifier in the second sense circuit of Claim 5. A transconductance amplifier is one that converts a voltage differential into a current source output. Nowhere does *Smith* mention "a transconductance differential amplifier." The Applicants have shown that *Smith* does not disclose the second sense circuit of Claim 5 and therefore cannot disclose the invention of Claim 14 further detailing the differential amplifier in the second sense circuit.

Therefore, the Applicants respectfully assert that the rejection of Claim 14 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 5.

Claim 15 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 15 further defines how the first ON-time pulse of Claim 1 is generated. The Applicants have shown that *Smith* does not disclose the invention of Claim 1 and therefore cannot disclose the invention of Claim 15 further detailing one of the limitations of Claim 1.

Therefore, the Applicants respectfully assert that the rejection of Claim 15 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 1.

Claim 16 is dependent from Claim 1 and contains all the limitations of Claim 1. Claim 16 further defines how the second ON-time pulse of Claim 1 is generated. The Applicants have shown that *Smith* does not disclose the invention of Claim 1 and

therefore cannot disclose the invention of Claim 16 further detailing one of the limitations of Claim 1.

Therefore, the Applicants respectfully assert that the rejection of Claim 16 under *35 U.S.C. § 102(b)* as being anticipated by *Smith* is traversed by the above arguments and for the same reasons as Claim 1.

II. REJECTION UNDER 35 U.S.C. § 103

The Examiner has rejected Claims 17-32 under *35 U.S.C. § 103(a)* as being unpatentable over *Smith* in view of U.S. Patent No. 6,429,628 to *Shin Nakagawa* (hereafter "*Nakagawa*").

Claims 17-32 are directed to a computer system that is powered by a power system having the multiphase buck regulator with peak current sharing disclosed in Claims 1-16. The Examiner states that *Smith* discloses the invention of Claim 17 but does not disclose a computer system also comprising one or more central processing units (CPUs), a memory for storing instructions and data for the CPUs, and a power system (as recited in Claim 1) for supplying power to the computer system. The Examiner relies on *Nakagawa* to teach these limitations of Claim 17 which he asserts are not disclosed by *Smith*.

The Applicants have shown that *Smith* does not disclose the invention of Claim 16. The Examiner does not state that *Nakagawa* teaches anything relative to the invention of Claim 16. While *Nakagawa* may teach aspects of powering a computer system, *Nakagawa* does not teach or suggest the particular power system of Claim 16 nor the combination of this power system and the computer system elements of Claim 17. Therefore, the Applicants assert that neither *Smith* nor *Nakagawa*, singly or in combination teach or suggest the invention of Claim 17.

Therefore, the Applicants respectfully assert that the rejection of Claim 17 under *35 U.S.C. § 103(a)* as being unpatentable over *Smith* in view of *Nakagawa* is traversed by the above arguments and for the same reasons as Claim 1.

The Examiner rejects Claims 18-32 for the same reasons as Claims 2-16. The Applicants have shown that *Smith* does not teach or suggest the inventions in Claims 2-16. The Examiner does not state that *Nakagawa* teaches or suggests anything relative to Claims 2-16. Therefore, the Applicants assert that *Smith* and *Nakagawa* do not teach or suggest, singly or in combination, the inventions of Claims 18-32.

Therefore, the Applicants respectfully assert that the rejections of Claims 18-32 under *35 U.S.C. § 103(a)* as being unpatentable over *Smith* in view of *Nakagawa* are traversed by the above arguments and for the same reasons as Claims 1 and 17.

III. CONCLUSION

The rejection of Claims 1-16 under *35 U.S.C. § 102(b)* over *Smith* have been traversed.

The rejection of Claims 17-32 under *35 U.S.C. § 103(a)* over *Smith*, in view of *Nakagawa* have been traversed.

As a result of the foregoing, it is asserted by Applicants that claims 1-32 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims.

Applicants respectfully request that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining problems.

Respectfully submitted,
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